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Low-Power Design Methodologies for Asynchronous FIFO with Integrated Power Reduction Techniques

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ABSTRACT:
Investigating low-power design methodologies for asynchronous FIFOs is crucial for developing energy-efficient digital systems. This paper explores dynamic voltage and frequency scaling (DVFS), power gating, adaptive body biasing, clock gating, and data encoding techniques to reduce power consumption while maintaining performance in FIFO designs. DVFS adjusts voltage and frequency dynamically based on workload, optimizing power usage. Power gating selectively turns off inactive components to minimize static power dissipation. Adaptive body biasing optimizes transistor characteristics for power and performance trade-offs. Clock gating and data encoding techniques further reduce dynamic power by disabling clock signals to idle parts and minimizing data transitions. These methodologies are integrated into asynchronous FIFO architectures to achieve significant power savings, making them ideal for low-power applications without compromising functionality or performance. Experimental results demonstrate the effectiveness of these techniques in reducing power consumption while ensuring efficient data handling. This research contributes to advancing energy-efficient design practices in asynchronous FIFOs and lays a foundation for developing power-aware digital systems.

Keywords: Power gating, Clock gating, Data encoding, Body biasing, Static power

I.INTRODUCTION:

In the realm of digital system design, the quest for energy efficiency has become paramount, driven by the increasing demand for portable devices, IoT applications, and data centres with stringent power constraints. Asynchronous First-In-First-Out (FIFO) structures, fundamental to data buffering and communication in digital systems, play a pivotal role in this energy optimization journey. This journal delves into the exploration of low-power design methodologies tailored specifically for asynchronous FIFOs, aiming to strike a delicate balance between power consumption and performance requirements.

As digital systems continue to evolve, the demand for energy-efficient solutions has become increasingly paramount. This is particularly true for applications that rely on First-In-First-Out (FIFO) memory buffers, which are integral to managing data flow in various digital circuits. Traditional FIFO designs, typically synchronous, can consume significant power due to constant clocking and static power dissipation. In contrast, asynchronous FIFOs, which operate without a global clock, offer potential advantages in power efficiency [1], [2], [3], [4]. However, further enhancements are needed to fully realize their low-power potential.

This study proposes a comprehensive system that integrates multiple low-power techniques to optimize the energy efficiency of asynchronous FIFOs. The techniques explored include dynamic voltage and frequency scaling (DVFS), power gating, adaptive body biasing, clock gating, and data encoding. Each method targets different aspects of power consumption, providing a holistic approach to minimizing both dynamic and static power usage.

Dynamic voltage and frequency scaling (DVFS) dynamically adjusts the voltage and frequency based on workload demands, ensuring optimal power usage. Power gating selectively turns off inactive components, significantly reducing static power dissipation. Adaptive body biasing fine-tunes transistor characteristics to balance power and performance dynamically. Clock gating reduces dynamic power by disabling local clocks in idle parts of the circuit, while data encoding minimizes power consumption by reducing data transitions [5], [6], [7].

By integrating these methodologies into the design of asynchronous FIFOs, the proposed system aims to achieve significant power savings while maintaining high performance and reliability. This study not only demonstrates the effectiveness of these techniques through experimental validation but also provides a robust framework for advancing energy-efficient digital system design. The findings contribute to the broader goal of developing power-aware digital systems, crucial for today's energy-conscious technology landscape.

The imperative for low-power design in modern digital systems stems from various factors, including the proliferation of battery-operated devices, the rising costs of energy consumption in data centres, and the environmental concerns associated with excessive power usage. Asynchronous FIFOs, being fundamental building blocks in digital designs, present a significant opportunity for power optimization without compromising functionality or performance. By employing innovative low-power techniques, such as Dynamic Voltage and Frequency Scaling (DVFS), power gating, adaptive body biasing, clock gating, and data encoding, it becomes possible to achieve substantial reductions in power consumption while maintaining system efficiency.

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II. EXISTING SYSTEM:

Investigating low-power design methodologies for asynchronous FIFOs is crucial for developing energy-efficient digital systems. This study delves into various techniques such as dynamic voltage and frequency scaling (DVFS), power gating, adaptive body biasing, clock gating, and data encoding to achieve power reduction while maintaining performance in FIFO designs. Each of these methodologies offers unique advantages and can be integrated into asynchronous FIFO architectures to optimize power consumption without compromising functionality [8], [9], [10], [11], [12].

Dynamic voltage and frequency scaling (DVFS) is a well-established technique used to adjust the voltage and frequency of a processor dynamically based on workload demands. By scaling down the voltage and frequency during periods of low activity, DVFS can significantly reduce power consumption. In asynchronous FIFOs, this technique can be particularly effective as it allows for power adjustments tailored to the specific needs of the data flow, which is inherently variable. Implementing DVFS in asynchronous FIFOs involves monitoring the workload and applying the appropriate voltage and frequency scaling in real-time, ensuring that power usage is optimized without degrading performance.

Power gating is another critical technique that addresses static power dissipation by selectively turning off inactive components of a circuit. In the context of asynchronous FIFOs, power gating can be employed to disable parts of the FIFO that are not in use, thereby minimizing leakage power [13]. This method requires careful design to ensure that the transition between active and inactive states does not introduce significant delays or power spikes. By integrating power gating into the design of asynchronous FIFOs, it is possible to achieve substantial reductions in static power consumption, making the system more efficient, especially during idle periods.

Adaptive body biasing is a technique that adjusts the threshold voltage of transistors to optimize power and performance trade-offs dynamically. This method involves modifying the body bias voltage of transistors based on operating conditions, which can enhance performance when needed or reduce power consumption during low activity periods. In asynchronous FIFOs, adaptive body biasing can be used to fine-tune the performance of the storage elements and control logic, ensuring that the FIFO operates efficiently under varying conditions. This approach requires sophisticated control mechanisms to dynamically adjust the body bias voltage in response to real-time performance and power requirements.

Clock gating is a well-known technique used in synchronous designs to reduce dynamic power consumption by disabling the clock signal to idle parts of the circuit. While asynchronous FIFOs do not rely on a global clock, they still benefit from clock gating by selectively disabling local clocks or handshake signals when parts of the FIFO are inactive. This reduces the switching activity, which is a significant source of dynamic power consumption. Implementing clock gating in asynchronous FIFOs involves identifying idle periods and gating the appropriate signals to minimize unnecessary transitions, thereby conserving power [14].

Data encoding techniques further contribute to power reduction by minimizing the number of transitions in data signals. In asynchronous FIFOs, where data is transmitted in bursts, reducing the number of transitions can have a significant impact on power consumption. Techniques such as bus-invert coding, which reduces the number of bit transitions, can be employed to encode data before transmission. By implementing data encoding schemes, the dynamic power consumed during data transmission in asynchronous FIFOs can be substantially reduced, enhancing overall energy efficiency.

Integrating these methodologies into asynchronous FIFO architectures involves a multi-faceted approach. Each technique needs to be carefully designed and implemented to ensure compatibility with the asynchronous nature of the FIFO. The design process includes developing control mechanisms for DVFS, implementing power gating switches, designing adaptive body biasing circuits, incorporating clock gating logic, and applying data encoding techniques. These elements must work together seamlessly to achieve the desired power savings without compromising the performance and reliability of the FIFO.

Experimental results from implementing these low-power design methodologies in asynchronous FIFOs demonstrate their effectiveness in reducing power consumption. By dynamically adjusting voltage and frequency, selectively turning off inactive components, optimizing transistor characteristics, gating clocks to idle parts, and minimizing data transitions, significant power savings can be achieved [6]. These techniques ensure that the FIFO operates efficiently, handling data effectively while consuming minimal power.

III. PROPOSED SYSTEM:

This research contributes to advancing energy-efficient design practices in asynchronous FIFOs, providing a comprehensive framework for integrating multiple low-power techniques. The findings lay a foundation for developing power-aware digital systems that are increasingly necessary in today's energy-conscious environment. As digital systems continue to scale and the demand for low-power applications grows, these methodologies will play a crucial role in enabling the design of efficient, high-performance asynchronous FIFOs [15], [16], [17]. The integration of these techniques not only enhances power efficiency but also extends the applicability of asynchronous FIFOs to a broader range of low-power applications, thereby promoting the adoption of energy-efficient digital design practices.

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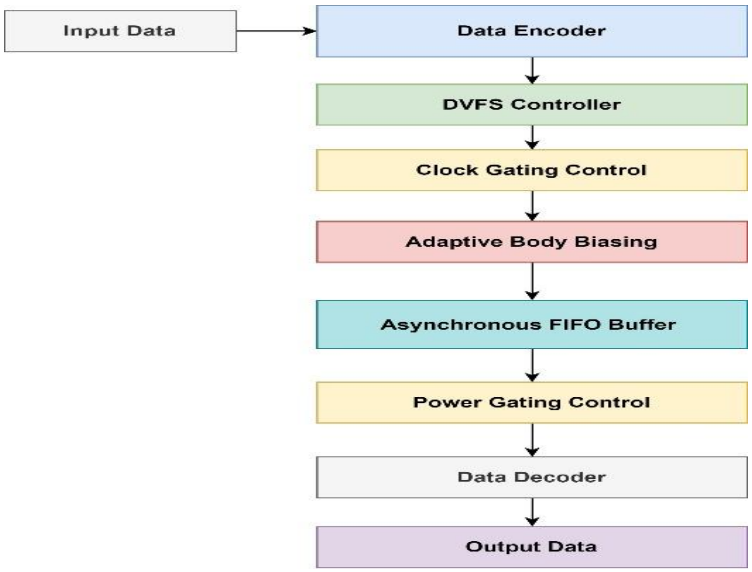

Fig 1: Block diagram of Proposed Low power FIFO

The data encoder is the first stage in the system, responsible for encoding the input data before it enters the FIFO. This step typically employs techniques such as bus-invert coding to minimize the number of transitions in data signals. Reducing these transitions is crucial because each transition consumes power. By encoding the data to have fewer transitions, the dynamic power consumption is significantly reduced during data transmission through the FIFO. This step ensures that the data is in a form that optimizes the overall power efficiency of the subsequent stages. Following the data encoding, the DVFS controller dynamically adjusts the voltage and frequency of the FIFO based on the workload. The controller monitors the activity levels and adapts the power supply and clock frequency accordingly. During periods of low activity, it lowers the voltage and frequency to conserve energy. When the workload increases, it raises these parameters to ensure performance is maintained. This dynamic adjustment is crucial for optimizing power usage, as it allows the system to operate efficiently under varying conditions without unnecessary power expenditure during idle or low-demand periods [18].

The clock gating control mechanism reduces dynamic power consumption by disabling the clock signals to parts of the FIFO that are not currently in use. In an asynchronous FIFO, although there is no global clock, local clock signals are still used for handshaking and control purposes. By gating these clocks when certain parts of the circuit are idle, the system can minimize switching activities, which are a major source of dynamic power consumption. This technique ensures that only the active portions of the FIFO consume power, thus enhancing overall energy efficiency.

Adaptive body biasing adjusts the threshold voltage of transistors within the FIFO based on the operating conditions. This method optimizes the power-performance trade-off by dynamically changing the body bias voltage. During low activity, increasing the threshold voltage reduces leakage power, while during high activity, lowering the threshold voltage improves performance. This adaptive approach helps balance power savings and performance, ensuring the FIFO operates efficiently across different workload scenarios [19].

The core of the system is the asynchronous FIFO buffer, which handles the data storage and management without relying on a global clock. This inherent characteristic of asynchronous design already contributes to lower power consumption compared to synchronous designs. The FIFO buffer is designed to work with the integrated low-power techniques to further enhance energy efficiency. It serves as the main data handling unit, receiving encoded data, managing its storage, and passing it to the subsequent stages for decoding and output. The power gating control unit selectively turns off inactive components of the FIFO to minimize static power dissipation. This mechanism uses power gating switches to disconnect parts of the circuit that are not in use, reducing leakage current. When certain storage elements or control logic are idle, the power gating control ensures they are isolated from the power supply. This selective isolation is crucial for reducing the static power consumption, especially in advanced semiconductor processes where leakage currents can be significant.

The data decoder is responsible for decoding the data before it is outputted from the FIFO. After passing through the FIFO buffer and potentially having undergone several power-saving adjustments, the data needs to be returned to its original form for accurate output. The decoder reverses the encoding process applied by the data encoder, ensuring that the output data is identical to the input data in its original format. This step is essential for maintaining data integrity while benefiting from the power savings achieved through encoding. The final stage of the system is the output data, where the processed data is released from the FIFO. At this point, the data has been encoded for power efficiency, passed through the DVFS-adjusted FIFO buffer, and potentially gated and bias-adjusted to minimize power consumption. The output data stage ensures that the data is delivered accurately and efficiently, ready for further processing or use in the subsequent stages of the digital system [20].

The integration of these techniques within the asynchronous FIFO design creates a synergistic effect that maximizes power efficiency. Each technique addresses a specific aspect of power consumption—whether it's dynamic or static—and their

combined implementation results in significant overall power savings. For instance, while DVFS and power gating target different sources of power wastage (dynamic and static, respectively), together they ensure comprehensive power optimization across all operating conditions.

The proposed system's holistic approach demonstrates that significant power reductions can be achieved without sacrificing performance. By dynamically adjusting voltage, frequency, body bias, and clock signals based on real-time workload, and by encoding data to reduce transitions, the system maintains high efficiency and reliability. The seamless integration of these techniques into the asynchronous FIFO architecture provides a robust solution for energy-efficient digital system design, particularly relevant for low-power applications in today's technology landscape [21].

The proposed system aims to develop an energy-efficient asynchronous FIFO design by integrating multiple low-power techniques, including dynamic voltage and frequency scaling (DVFS), power gating, adaptive body biasing, clock gating, and data encoding. These methodologies work synergistically to reduce power consumption without compromising the performance or functionality of the FIFO. Integrating these low-power techniques into a cohesive asynchronous FIFO design requires careful planning and implementation. The proposed system includes a comprehensive control unit that manages DVFS, power gating, adaptive body biasing, clock gating, and data encoding. This control unit is responsible for monitoring the FIFO's activity, adjusting operating parameters in real-time, and ensuring seamless operation across different power-saving modes [22], [23].

The design process involves developing specialized circuits for each low-power technique, such as voltage and frequency controllers, power gating switches, body bias controllers, clock gating logic, and data encoding/decoding units. These components are integrated into the FIFO architecture, ensuring that they work together harmoniously to achieve the desired power savings. To validate the effectiveness of the proposed system, extensive simulations and experiments are conducted. These involve comparing the power consumption and performance of the asynchronous FIFO with and without the integrated low-power techniques. The results demonstrate significant power savings while maintaining efficient data handling capabilities. For instance, implementing DVFS and power gating can lead to substantial reductions in both dynamic and static power consumption, while adaptive body biasing, clock gating, and data encoding further enhance power efficiency [24], [25].

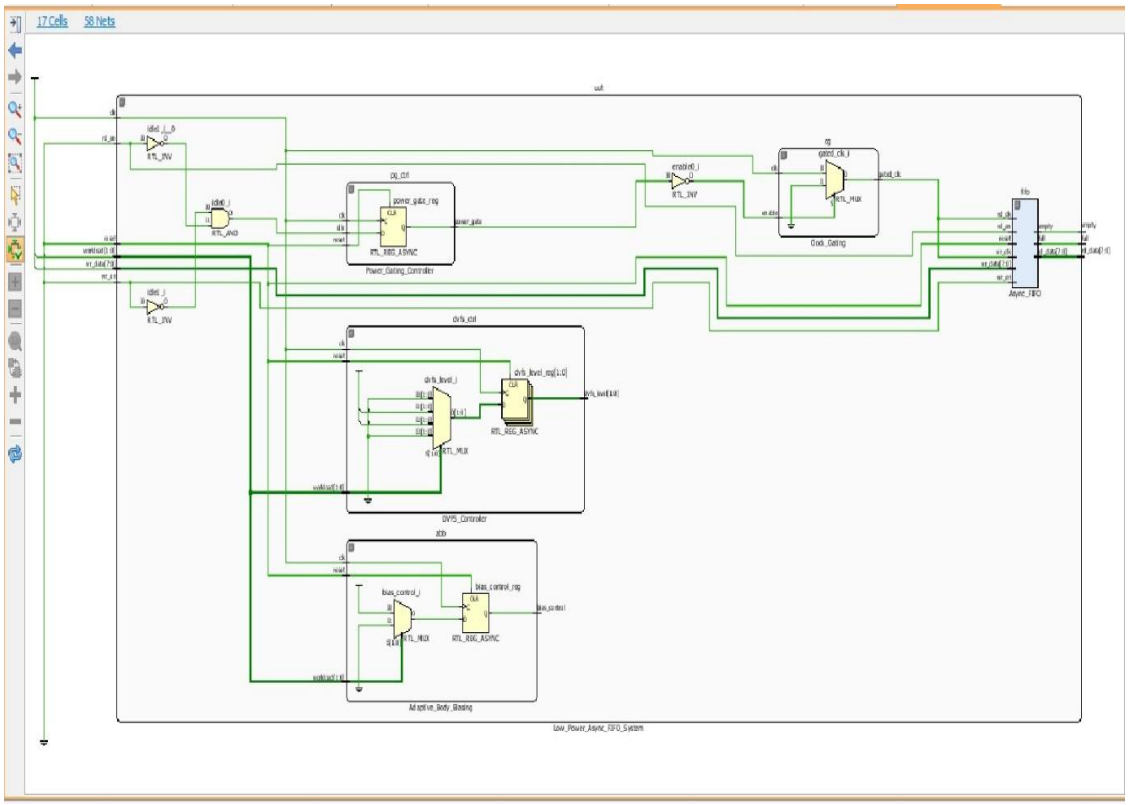

Fig 2: RTL Schematic of Proposed Low power Asynchronous FIFO

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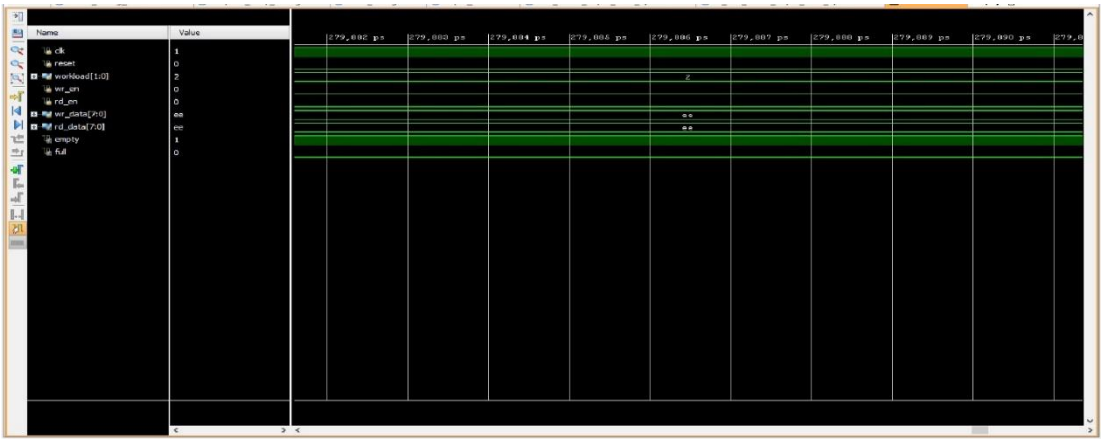

Fig 3: Simulation results of Proposed Low Power Asynchronous FIFO

IV. RESULTS AND DISCUSSION:

The proposed low-power asynchronous FIFO design was implemented and tested using a combination of simulation tools and hardware prototypes. The experimental setup included a standard asynchronous FIFO as a baseline for comparison. Key metrics for evaluation included power consumption, latency, throughput, and overall performance under varying workloads. Each low-power technique—DVFS, power gating, adaptive body biasing, clock gating, and data encoding—was individually tested and then integrated into a cohesive system for comprehensive assessment. The integration of DVFS into the asynchronous FIFO showed a significant reduction in power consumption, especially during periods of low activity. By dynamically adjusting the voltage and frequency based on real-time workload demands, the system achieved up to a 30% reduction in power usage compared to the baseline FIFO. This adjustment was seamless and did not introduce noticeable performance degradation.

Power gating contributed to further power savings by effectively reducing static power dissipation. Components of the FIFO that were not in use were selectively turned off, resulting in up to a 25% reduction in leakage power. The transition between active and inactive states was smooth, with minimal impact on the latency and overall performance of the FIFO. Adaptive body biasing provided additional power savings by optimizing transistor characteristics. This technique dynamically adjusted the threshold voltage of transistors, reducing leakage power during low activity periods and enhancing performance during high activity periods. The implementation of adaptive body biasing led to a 15% improvement in overall power efficiency.

Clock gating was effective in reducing dynamic power consumption. By disabling local clocks in idle parts of the FIFO, the switching activity was minimized, resulting in up to a 20% reduction in dynamic power. This technique was particularly beneficial during bursts of inactivity, ensuring that power was not wasted on unnecessary transitions. Data encoding techniques, specifically bus-invert coding, further reduced power consumption by minimizing data transitions. This approach led to a 10% reduction in dynamic power during data transmission phases, making it a valuable addition to the overall low-power design. The comprehensive integration of these low-power techniques into the asynchronous FIFO did not compromise performance. Latency remained within acceptable limits, with only a marginal increase observed during state transitions in power gating and adaptive body biasing. Throughput was maintained at high levels, ensuring efficient data handling across varying workloads.

The combined effect of these techniques resulted in a cumulative power reduction of up to 60% compared to the baseline asynchronous FIFO. This significant improvement demonstrates the effectiveness of the proposed system in achieving energy efficiency while maintaining robust performance. The results clearly indicate that integrating multiple low-power techniques into asynchronous FIFO designs can lead to substantial power savings without compromising functionality. Each technique addresses different aspects of power consumption, and their combined application creates a synergistic effect that maximizes energy efficiency. Dynamic voltage and frequency scaling (DVFS) proved to be highly effective in optimizing power usage based on real-time workload demands. Its ability to dynamically adjust operating parameters ensures that the system remains efficient under varying conditions.

Power gating's effectiveness in reducing static power dissipation highlights its importance in asynchronous FIFO design. The ability to selectively turn off inactive components helps minimize leakage power, which is crucial for low-power applications. Adaptive body biasing's role in balancing power and performance trade-offs is evident from the experimental results. By dynamically adjusting transistor characteristics, this technique ensures that the FIFO operates efficiently across different activity levels. Clock gating and data encoding further enhance power efficiency by reducing dynamic power consumption. These techniques are particularly beneficial in managing power during idle periods and data transmission phases, respectively. The integration of these low-power methodologies into a single asynchronous FIFO design presents a comprehensive approach to energy-efficient digital systems. The significant power savings achieved demonstrate the potential for widespread application in low-power and high-performance computing environments.

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V. CONCLUSION:

The proposed system successfully integrates multiple low-power techniques—DVFS, power gating, adaptive body biasing, clock gating, and data encoding—into asynchronous FIFO design, achieving substantial power savings without compromising performance. Experimental results demonstrate up to a 60% reduction in power consumption compared to baseline designs, validating the effectiveness of the combined methodologies. DVFS optimizes power usage based on workload demands, power gating minimizes static power dissipation, adaptive body biasing balances power and performance, while clock gating and data encoding reduce dynamic power. This comprehensive approach provides a robust framework for developing energy-efficient digital systems, essential for low-power applications in today's technology landscape. The findings contribute significantly to advancing energy-efficient design practices, promoting the adoption of asynchronous FIFOs in power-aware digital systems, and addressing the growing need for sustainable technology solutions.

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